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Fig.1

PRIOR ART

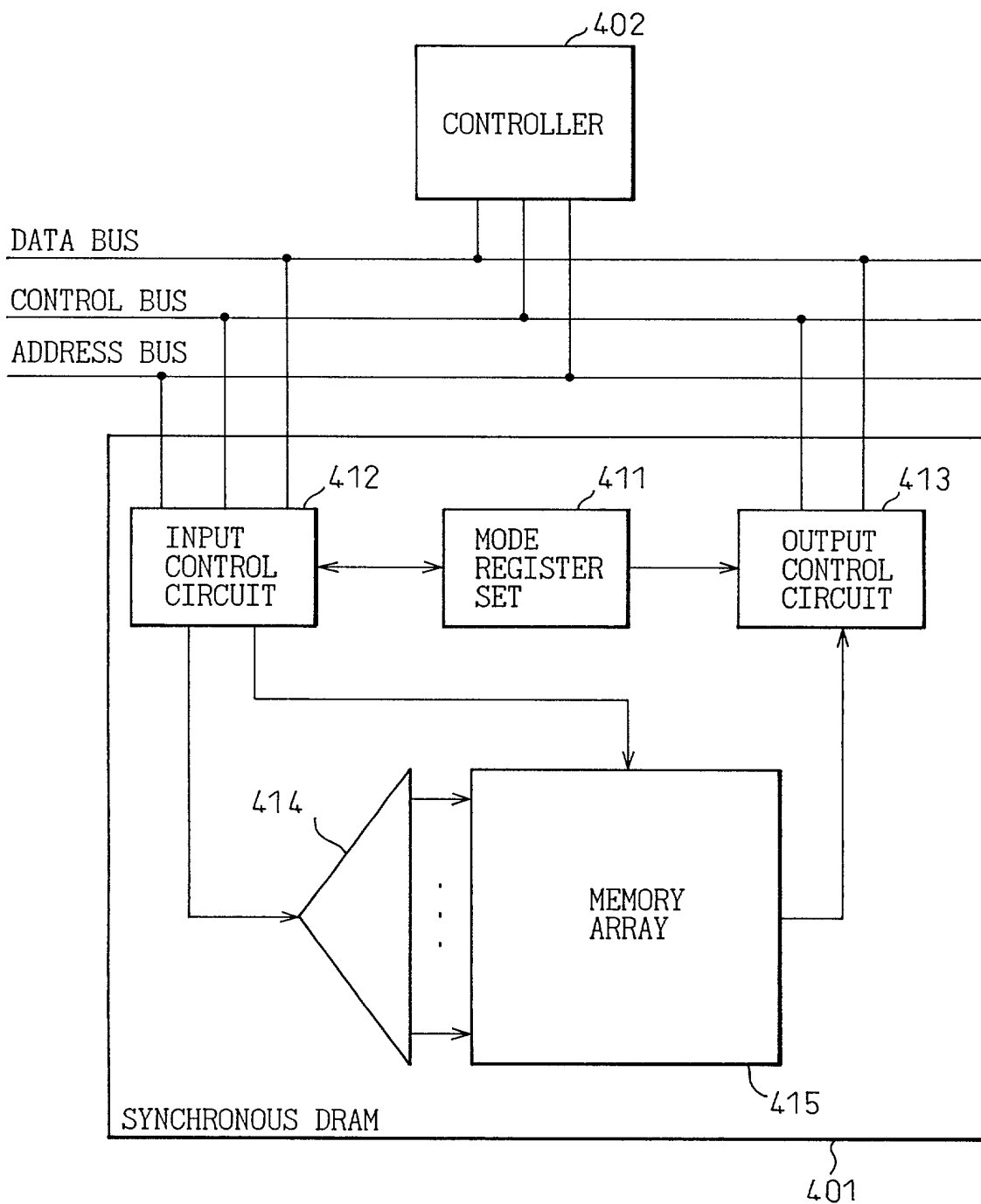


Fig.2

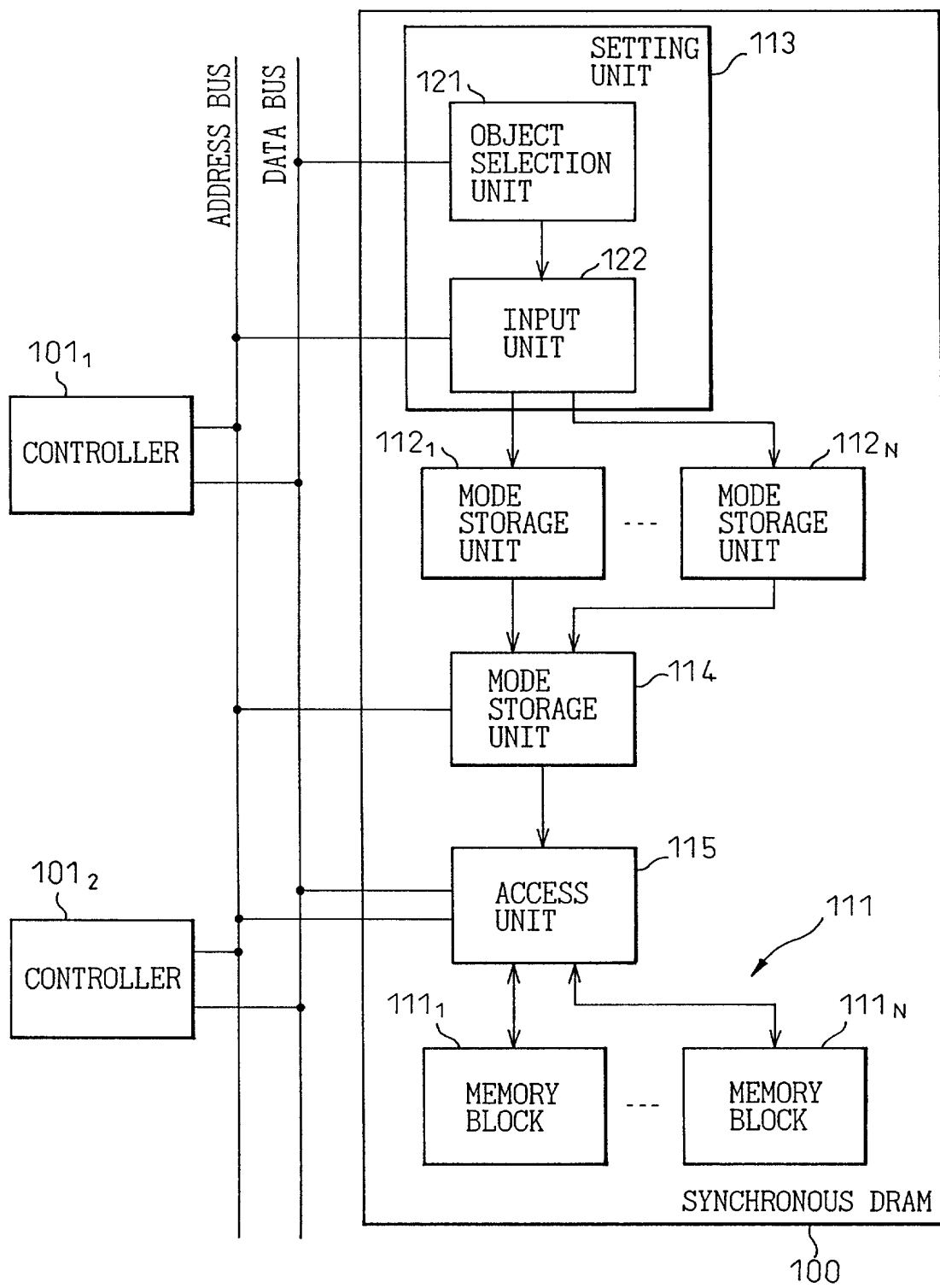


Fig.3

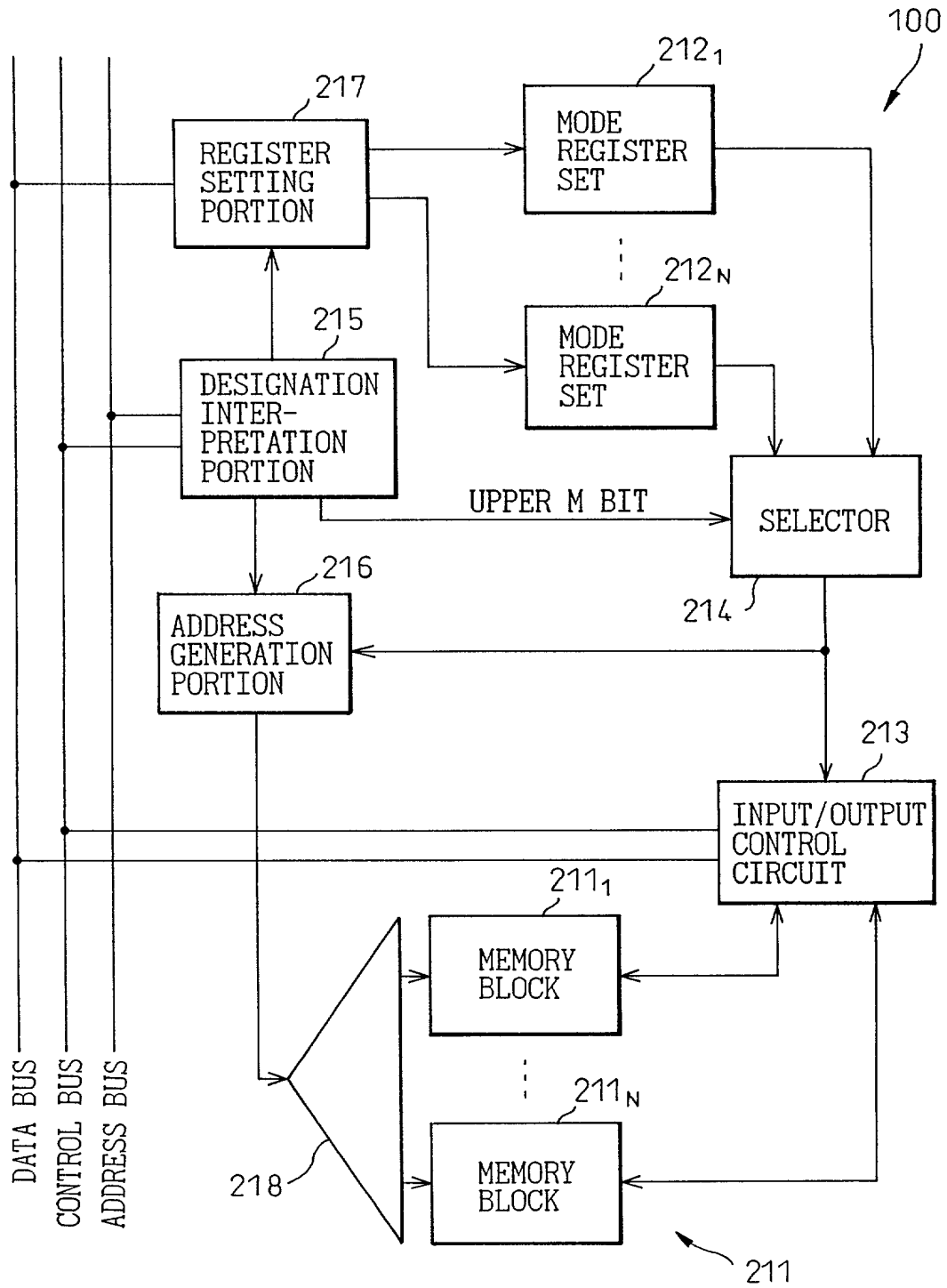


Fig.4

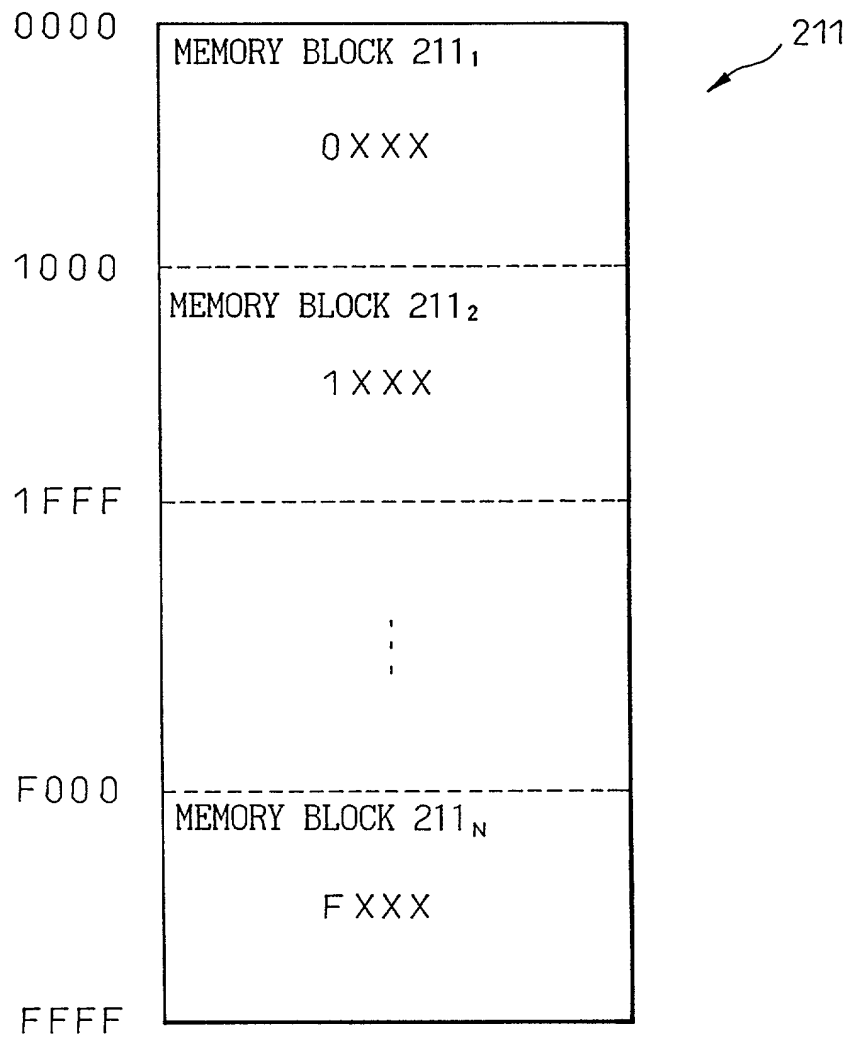


Fig.5A

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
WBL		TEST MODE		CAS LATENCY		BT	BURST LENGTH		

WBL: WRITE BURST LENGTH  
BT: BURST TYPE

Fig.5D

TEST MODE

A8	A7	
0	0	OPERATION MODE SETTING
0	1	SPARE
1	0	SPARE
1	1	SPARE

CAS LATENCY

A6	A5	A4	
0	0	0	SPARE
0	0	1	2
0	1	0	3
0	1	1	SPARE
⋮	⋮	⋮	⋮
1	1	1	SPARE

Fig.5B

BURST LENGTH

A2	A1	A0	BT = 0	BT = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	SPARE	SPARE
⋮	⋮	⋮	⋮	⋮
1	1	1	FULL BURST	SPARE

Fig.5E

A9	WBL
0	BURST
1	SINGLE BIT
A3	BT
0	SEQUENTIAL
1	INTERLEAVE

Fig. 6A

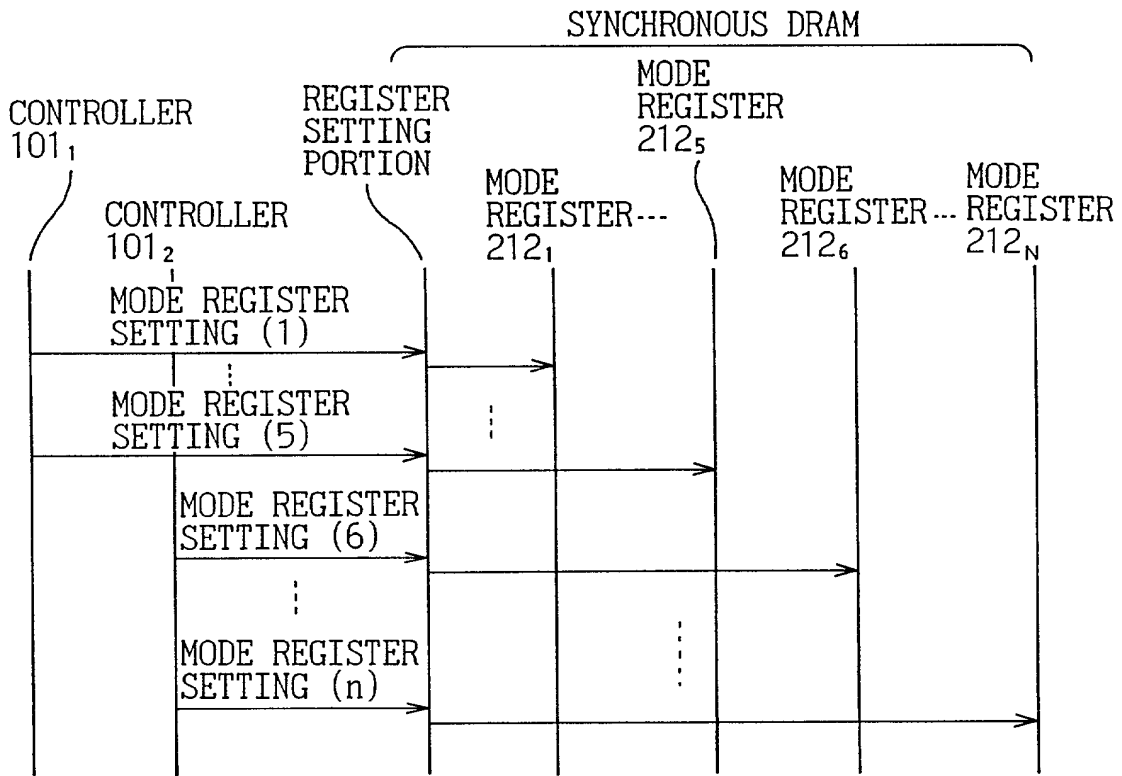
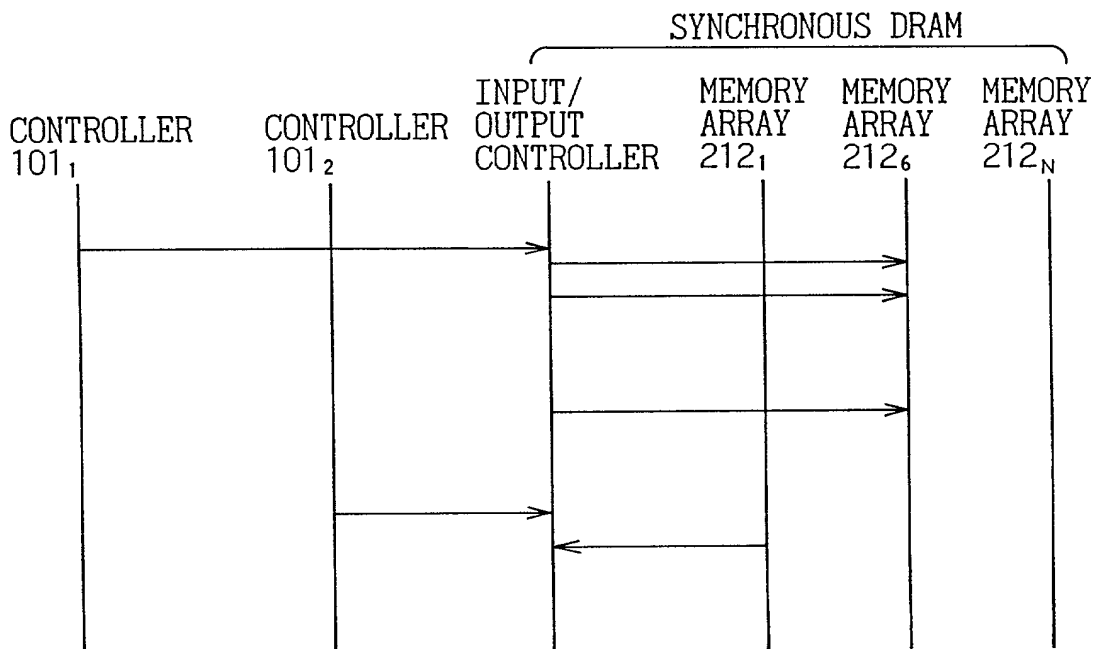


Fig. 6B



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Fig.7

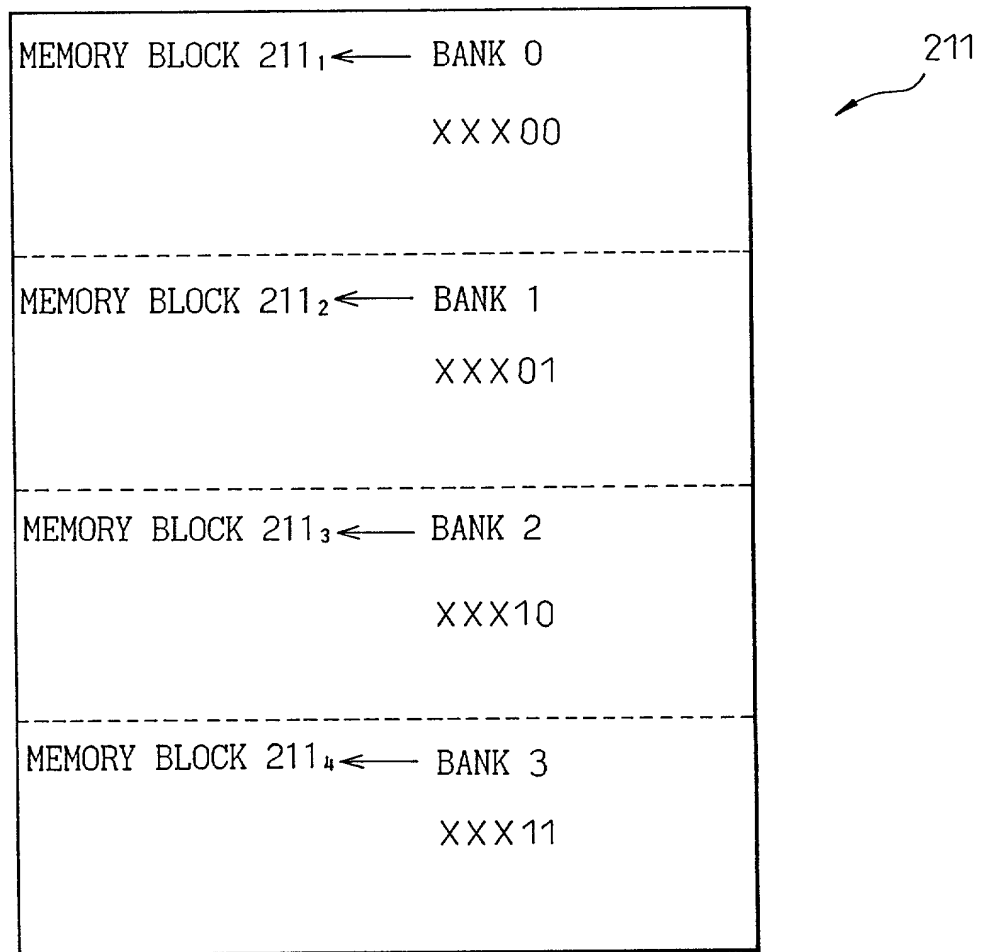


Fig.8

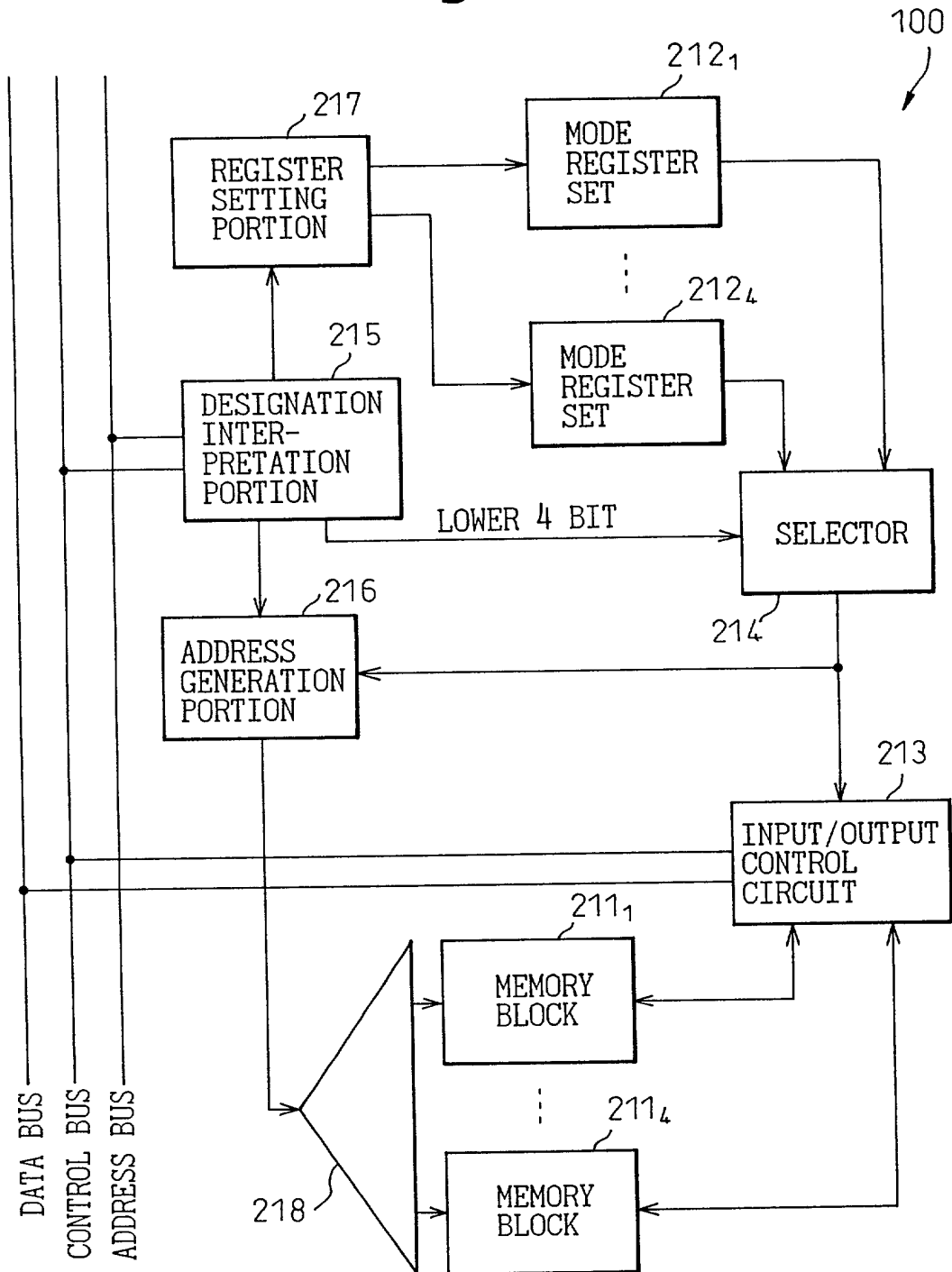




Fig.9

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
WBL	TEST MODE		CAS LATENCY			BT	BURST LENGTH		

WBL: WRITE BURST LENGTH  
BT: BURST TYPE

TEST MODE

A8	A7	
0	0	OPERATION MODE SETTING (1)
0	1	OPERATION MODE SETTING (2)
1	0	OPERATION MODE SETTING (3)
1	1	OPERATION MODE SETTING (4)